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WORLD'S #1 ACADEMIC OUTLINE

Quick Study® ACADEMIC

ELECTRONICS 1 PART TWO 2

PART 2 of FUNDAMENTALS OF ELECTRONIC DEVICES & BASIC ELECTRONIC CIRCUITS

OPERATIONAL AMPLIFIERS

DEFINITIONS

- A basic differential amplifier (see Electronics Chart *Part One*) enables mathematical difference operation and can be modified to perform addition, integration and differentiation. Hence, the differential amplifier is also designated as an **Operational Amplifier** (Op-Amp).

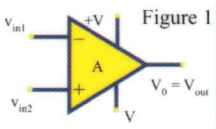


Figure 1

- An Op-Amp represents, in essence, a high-gain electronic circuit intended to amplify the difference in the signal voltages applied to its two input terminals, namely, inverting (–) and non-inverting (+) inputs (see Fig. 1).

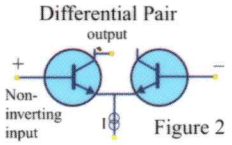


Figure 2

- In simple form (Fig. 2), an Op-Amp constitutes a differential amplifier made up of, for example, a pair of BJTs driven by a constant current source (**I**). JFETs and MOSFETs can also be used as differential pairs.

IDEAL OP-AMP CHARACTERISTICS

- Nominal voltage gain, $\mathbf{A} \rightarrow \infty$
- Input impedance (at both inputs), $\mathbf{Z_{in}} \rightarrow \infty$
- Output impedance, $\mathbf{Z_0} \rightarrow \mathbf{0}$
  - Both transistors are identical.
  - $\mathbf{v_0 = -Av_{in1} = Av_{in2}}$; or, if $\mathbf{v_{in1} = v_{in2}}$, $\mathbf{v_0 = 0}$
  - Bandwidth **(BW)** $\rightarrow \infty$
  - With bipolar transistors, it may be difficult to achieve a very high-input impedance.
- JFET and MOSFET provide high-input impedance capabilities.

OP-AMP OPERATIONAL PARAMETERS

In reference to typical inverting (Fig. 3, above right) and non-inverting (Fig. 4) modes of operational characteristics:

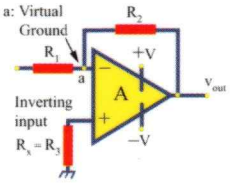
- **INPUT BIAS CURRENT**: This is the emitter current in the differential amplifier for active region operation of the pair of BJTs (e.g. **0.05μA for 741 OP-AMP**) which comes through $\mathbf{R_2}$ so that $\mathbf{v_{out} = (0.05 \times 10^{-6} \times R_2)}$volts. This could be large enough to saturate the output. Saturation is overcome by introducing $\mathbf{R_x = R_1 \parallel R_2}$ and made adjustable to compensate for input offset current due to any dissimilarities in the differential pair configuration (Fig. 3).
- **INPUT OFFSET VOLTAGE** ($\approx \pm$ **60mV**): It is required at the input as a counter voltage to offset the finite unbalance voltage due to unequal current flowing through the differential pair devices in the OP-AMP, so that this balancing gives zero output voltage.
- **CMRR**: When the OP-AMP is ideally balanced at the input, the output voltage = 0, i.e. $\mathbf{v_{in1} = v_{in2}}$, and this circuit can reject common-mode signals due to its common-mode gain $\mathbf{(A_c) = 0}$. For differential mode signals $\mathbf{(v_{in1} - v_{in2})}$, the gain $\mathbf{(A_d)} \rightarrow \infty$. The ratio $\mathbf{A_d/A_c}$ **common-mode rejection ratio** (CMRR). In practical OP-AMPs, $\mathbf{A_c > 0}$ and $\mathbf{A_d < \infty}$; or, CMRR is finite and indicates the extent of balance in the OP-AMP (A figure of merit parameter).
  - **OUTPUT VOLTAGE SWING**: This is the peak output swing with reference to zero at the output. It is limited by power supply voltages used ($\approx$ 80 percent of power supply voltage $\pm$ V).
- **INPUT VOLTAGE SWING**: Input common-mode voltage swing is limited by the saturation of the differential amplifier at the input: ($\approx$ 30 percent of power supply voltage $\pm$ V).
- **SLEW RATE**: Maximum rate at which the output voltage can change (volts/microsecond). In ideal OP-AMPs, slew-rate $\rightarrow \infty$.
- **OTHER PARAMETERS**: (1) Bandwidth; (2) Maximum output current available when the output terminal is set to ground; (3) PSRR: Power supply rejection ratio: Change in input offset voltage to corresponding change in one of the power supply voltages ($\pm$V). Ideally, PSRR = 0; in practice, it is of the order of a few μV/V.

FREQUENCY ROLL-OFF

It is the fall-off of the voltage gain at high frequencies. This is indicated by gain-bandwidth product. Roll-off to higher frequencies is achieved by frequency compensation.

INVERTING AMPLIFIER (VIRTUAL GROUND AMPLIFIER)

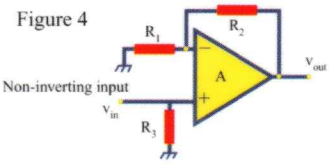
Figure 3



- Output impedance with feedback $\equiv \dfrac{\text{Output impedance of the OP-AMP} \times \text{Closed-loop gain}}{\text{(Open - loop gain)}}$
- Node **a** is almost at ground potential.
- Closed-loop voltage gain $\mathbf{v_{out} / v_{in} = -R_2/R_1}$
- Input impedance = $\mathbf{R_1}$
- Output impedance = $\mathbf{R_0}$

NONINVERTING AMPLIFIER

Figure 4



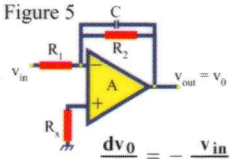
$\mathbf{A_V = 1 + \dfrac{R_2}{R_1}}$

$\mathbf{Z_{in} = R_3}$

$\mathbf{Z_{out} \rightarrow Low}$

INTEGRATOR (LOW-PASS FILTER)

Figure 5



- $\mathbf{R_2}$: Provides negative feedback for low-output impedance needs, but it also distorts the output.

$$\frac{dv_0}{dt} = -\frac{v_{in}}{R_1 C} \quad v_0 = -\left(\frac{1}{R_1 C}\right) \times \int v_{in}\, dt$$

DIFFERENTIATOR (HIGH-PASS FILTER)

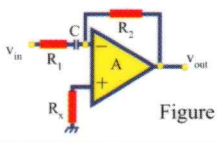


Figure 6

- Inverse operation of the integrator circuit.

LEVEL CLAMPING

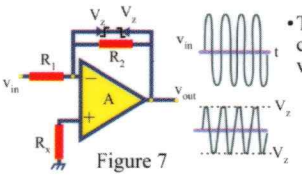
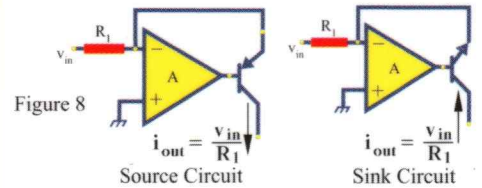


Figure 7

- The output is clamped to Zener voltage $\mathbf{V_z}$.

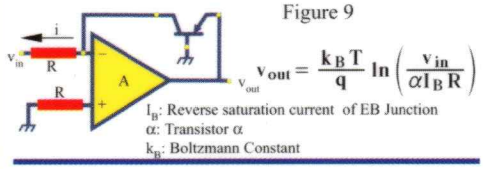
LINEAR VOLTAGE-TO-CURRENT CONVERTERS

Figure 8



LOGARITHMIC AMPLIFIER

Figure 9

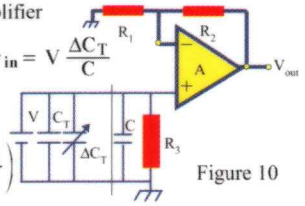


CHARGE AMPLIFIER

Charge Amplifier

Input (from a capacitive transducer): $v_{in} = V \dfrac{\Delta C_T}{C}$

C_T: Nominal capacitance of the transducer charged by a voltage V.



$\mathbf{v_{out} = v_{in}\left(1 + \dfrac{R_2}{R_1}\right)}$

Figure 10

PRECISION RECTIFIER & PEAK DETECTOR

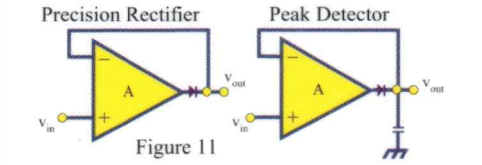
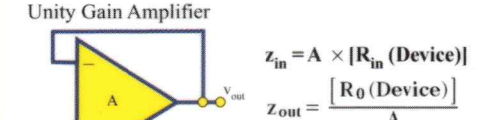


Figure 11

VOLTAGE FOLLOWER (UNITY GAIN AMPLIFIER)

Unity Gain Amplifier



$\mathbf{z_{in} = A \times [R_{in}\ (Device)]}$

$\mathbf{z_{out} = \dfrac{[R_0\ (Device)]}{A}}$

Figure 12

The output voltage "follows" the input voltage. Used as a buffer amplifier with high-input/low-output impedance realization.

REGULATED POWER SUPPLY

The Zener diode offers a constant reference voltage $\mathbf{(V_z)}$. Bias derived from the unregulated voltage $\mathbf{(V_B)}$, via potential division by $\mathbf{R_1}$ and $\mathbf{R_2}$ and the Zener reference voltage, are compared by an inverting amplifier to provide a stable output voltage.

$\mathbf{v_{out} = V_z\,(1 + R_1 / R_2)}$ and $\mathbf{I_z = (v_{out} - V_z) / R_3}$

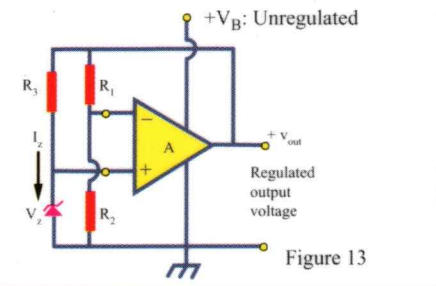


Figure 13

UNIPOLAR DEVICES FIELD EFFECT TRANSISTORS (FETs)

DEFINITIONS

- The device current is decided by one type of current carrier only (unipolar).
- The device interior current is controlled by an electric field applied in the path of the current carriers.

FET TYPES

- **JFET (Junction Field Effect Transistor)**: In the JFET, the resistance of the current path is modulated by the application of bias voltages to **PN** junctions adjacent to it.
- **MOSFET (Metal-Oxide Semiconductor FET)**: In MOSFET, there are no junctions. The controlling electric field is applied *via* an insulating layer to regulate the resistance of a main conducting path.

FET OPERATION MODES

- **Depletion mode operation**: The controlling electric field reduces the number of carriers available for conduction.
- **Enhancement mode operation**: Application of electric field causes an increase in the majority-carrier density in the conducting regions of the transistor.

JFET: DEVICE OPERATION

JFET: Device Operation

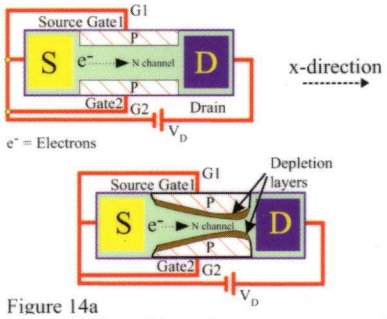


Figure 14a

Due to the application of the voltage across **source (S)-to-drain (D)**, electrons flow from **S** to **D** (majority carrier flow). The path between **S**-to-**D** has an ohmic resistance. Therefore, flow of electron current would cause a voltage drop and the potential at any point along this path (x-direction) increases from the source to drain (becoming more positive towards the drain end). Since the gates (tied together) are connected to the source, the N-region of the **channel** and the regions of the **gate** would form a reverse-biased PN junction. The extent of reverse bias increases progressively from the source side to drain side. Correspondingly, the depletion layers formed will be wider near the drain side as shown. Normally, the P-type gates (G_1 and G_2) are heavily doped relative to the N-channel region. Therefore, channel has (relatively) high resistance. Hence, the depletion layer widens predominantly into the channel region. Suppose V_D is increased. Consequently, the depletion layer into the channel widens more. As a result, eventually the two (top and bottom) depletion layers meet each other. Therefore, the channel is closed, not permitting the flow of electrons through it. This condition is known as **pinch-off**.

OUTPUT CHARACTERISTICS OF JFET

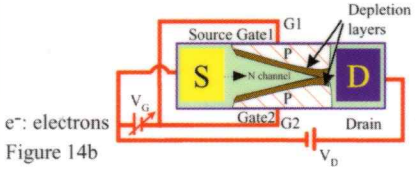


Figure 14b

Suppose an additional bias V_G is applied between the gates and the source terminals (Figure 14b):

- Suppose, $V_G = 0$. In the absence of drain current, the depletion layer is uniform along the channel. As V_D increases, I_D increases. Corresponding voltage drop along the channel causes a wedge-shaped path due to reasons discussed before. Upon pinch-off, the drain current remains constant at a saturated value.
- When V_G is applied: This provides additional reverse-bias. Therefore, pinch-off will occur at lower V_D and the corresponding $V_{D(sat)}$ will also be smaller. Hence, application of V_G modulates the channel dimension and reduces I_D. This is a depletion mode operation. Channel current decreases as the gate voltage is increased.

LINEAR OPERATION OF JFET

Linear Operation of JFET

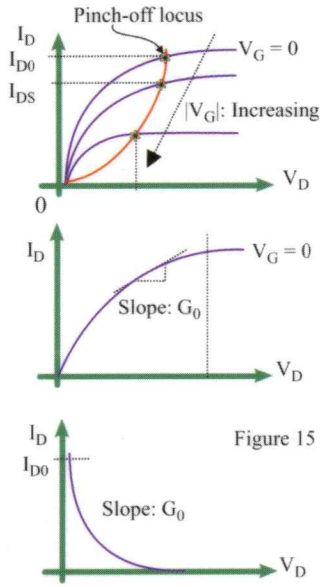


Figure 15

Suppose channel is lightly doped relative to the gates, i.e. $N_{a(gate)} >> N_{d(channel)}$. ∴ Thickness of depletion layer in the N-channel is $d_n \cong \left[\frac{2\varepsilon (V_0 + V_G)}{eN_D}\right]^{\frac{1}{2}}$. ∴ As V_G changes, d_n changes.

[V_0: Contact potential, N_a and N_d are acceptor and donor concentrations; ε: Permittivity of the channel].

Let V_{P0} be the value of V_G at which pinch-off occurs. The corresponding **change in $I_D = 0$**. For $V_G < V_{P0}$,

$$I_D \approx G_0 \left[1 - \left(\frac{V_G}{V_{P_0}}\right)^{\frac{1}{2}}\right] V_D,$$

where G_0 = **channel conductance** with zero bias (V_G = **0**) condition:

$$G_0 = (eN_d\mu_e) \times$$

[Area of cross-section of the channel / Length of the channel]

e: electronic charge; μ_e: electron mobility.

JFET OPERATION

Upon pinch-off:

$$I_{DS} = I_{D_0}\left[1 - \frac{3V_G}{V_P} + 2\left(\frac{V_G}{V_P}\right)^{\frac{3}{2}}\right]$$

Transfer Characteristics:

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_G}\right|_{V_D} = -I_{D_0}\frac{3V_D}{V_P^2}\left[1 - \left(\frac{V_G}{V_P}\right)^{\frac{1}{2}}\right]$$

g_m ≙ Mutual/transfer conductance

$$= \textbf{Max } g_m = g_m\big|_{V_G = 0} = g_{m_0} = \frac{-3I_{D_0}}{V_P} = -G_0$$

= Conductance of the channel with zero bias

$$g_m \cong g_{m_0}\left[1 - \left(\frac{V_G}{V_P}\right)^{\frac{1}{2}}\right]$$

MOSFET

DEFINITIONS

⇒ Induced channel device/Insulated Gate FET (IG FET)

- The gate is totally insulated from the semiconductor by a thin layer of SiO_2.
- The voltage applied at the gate induces a conducting channel within the semiconductor and modulates its conductivity.

ENHANCEMENT TYPE MOSFET

Enhancement-type MOSFET

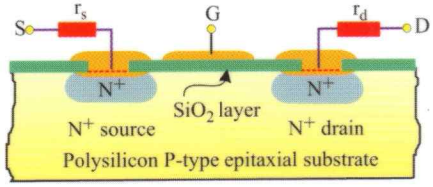


Figure 16

SiO_2⇒100 to 300 A° (Thermally grown insulation layer)

MOSFET Operation

No gate bias

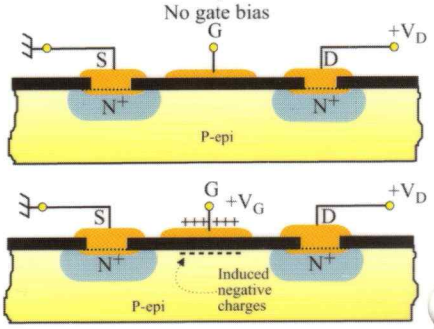


Figure 17

MOSFET OPERATION

Suppose no gate voltage is applied. Then N^+P junction at the source, as well as PN^+ junction at the drain, are reverse-biased. Therefore, no drain current flows. Suppose a small $+V_G$ is applied at the gate. The positive voltage at the top of the SiO_2 dielectric would induce negative charges below this layer. These negative charges will deplete the holes of the P-epilayer, exposing negatively charged acceptor ions, i.e. a depletion layer will be formed just below the gate as shown in Fig. 17. A further increase in $+V_G$ will induce more and more negative charges below the gate, with the result being a copious accumulation of negative charges below the gate forming an induced-layer of negative charges constituting a **"channel" (induced channel)** between the source and the drain as shown in Fig.18.

N-type Induced Channel

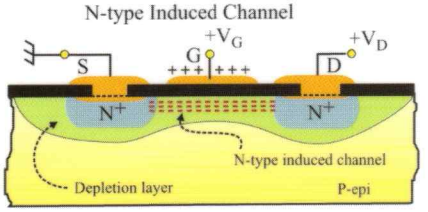


Figure 18

Once the channel is induced between the **S** and **D**, the electrons flow through this channel, with the result being a drain current. Therefore, the induced channel constitutes an ohmic path. The conductivity of this channel is dependent on the magnitude of V_G. In other words, the channel conductivity is modulated by V_G. Therefore, the more the V_G, the more will be I_D. Thus, the device operates in enhancement mode.

MOSFET OUTPUT CHARACTERISTICS

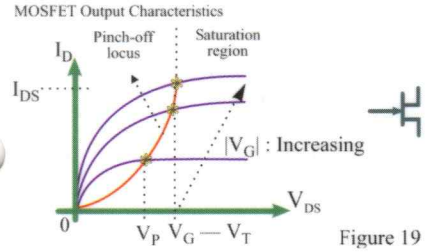


Figure 19

Analysis: Let voltage at x along the channel be $\mathbf{V(x)}$.

$$I_D = \left(\frac{\mu_e C_g}{L^2}\right)\left(V_G - V_T - V_D/2\right)V_D \Rightarrow$$ This $\mathbf{I_D}$ versus $\mathbf{V_D}$ is valid as long as $\mathbf{V_G - V(x) > V_T}$. Note: **L** : Channel length. At some gate voltage $\mathbf{V_{G_1}}$ with $\mathbf{V(x) = V_D}$, the channel is turned open and the flow of charges along the channel becomes constant, i.e. at $\mathbf{V_D = V_{G1} - V_T}$,

$$I_{ds} = \frac{\left(\frac{\mu_e C_g}{L^2}\right)\left(V_{G1} - V_T\right)^2}{2}$$

$$\left.\frac{\partial I_D}{\partial V_G}\right|_{V_D} \Rightarrow g_m = \mu_e C_g \frac{V_D}{L^2}$$

≙Transconductance of the MOSFET

$$I_{DS} = I_D\big|_{V_D = V_G - V_T} = \frac{\mu_e C_g}{2L^2}\left(V_G - V_T\right)^2 = g_m \frac{V_D}{2}$$

V-I CHARACTERISTICS OF ENHANCEMENT-TYPE MOSFET

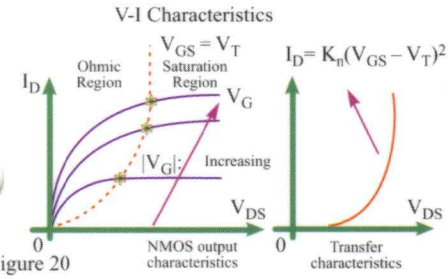


Figure 20

- **Ohmic Region (Triode Region)**

Here $\mathbf{V_{DS} \le V_{GS} - V_T}$ and the **V-I** characteristic is

$\mathbf{I_D = K_n|2(V_{GS} - V_T)V_{DS} - V^2_{DS}|}$, where

$$K_n = \frac{\mu_e \varepsilon_o \varepsilon_{ox}}{2t_{ox}}\frac{W}{L} = \frac{\mu_e C_{ox}}{2}\left(\frac{W}{L}\right)$$ and μ_e = surface mobility of electrons: $\mu_e = 800 cm^2$ / volt-sec (in Si).

ε_o = permittivity of free space **(= 8.85 x 10 $^{-14}$ F/cm)**

ε_{ox} = dielectric constant of SiO_2 ($\cong 4$);

$\mathbf{t_{ox}}$ = thickness of the oxide; $\mathbf{C_{ox} = \varepsilon_o \varepsilon_{ox} LW/t_{ox}}$

$\mathbf{C_{ox}}$: Capacitance of SiO_2 layer

Dividing locus between saturation and ohmic regions is given by substituting $\mathbf{V_{DS} = (V_{GS} - V_T)}$:

$$\mathbf{I_D = K_n V^2_{DS} = \frac{\mu_e C_{ox} W}{2L} V^2_{DS}}.$$

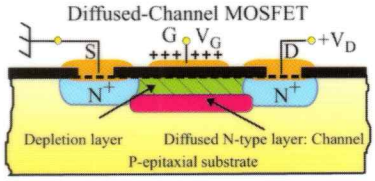
This locus is shown by the dotted line in Figure 20.

- **SATURATION REGION**: Here, $\mathbf{V_{DS} \ge V_{GS} - V_T}$, and the current $\mathbf{I_D}$ is approximately constant as shown in Fig. 20. The transfer characteristic is obtained by replacing $\mathbf{V_{DS}}$ by $\mathbf{V_{GS} - V_T}$: $\mathbf{I_D = K_n (V_{GS} - V_T)^2}$. A plot of the transfer characteristic is shown in Fig. 20.
- **CUTOFF REGION**: Here, $\mathbf{V_{GS} < V_T}$, and thus $\mathbf{I_D = 0}$. The device is *OFF* in this region and is used in switching applications in this mode.

DIFFUSED-CHANNEL (DEPLETION-TYPE) MOSFET

- Diffused-channed MOSFET can be operated both as depletion mode or as enhancement mode device.
- The device has a thin N-type layer of the same conductivity as source or drain and is diffused below the gate.

- When the gate has a small negative bias, the resulting positive charges in this diffused region cause the depletion layer (channel conductance) to be reduced. Thus, negative bias on gate enables depletion mode operation.



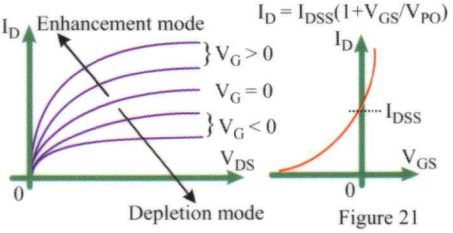


Figure 21

- When a positive bias is applied, more electrons are drawn into the channel causing more carrier population, i.e. channel conductance is increased. Hence, more current would flow; or, an increase in $+\mathbf{V_G}$ would increase $\mathbf{I_D} \Rightarrow$ *enhancement mode operation*. **V–I** characteristics indicate that circuit operations of diffused channel MOSFET are similar to those of JFET.

SMALL-SIGNAL EQUIVALENT CIRCUIT & FREQUENCY RESPONSE OF FETs

Normal symbolic representations of the JFETs and the MOSFETs are shown in Fig. 22.

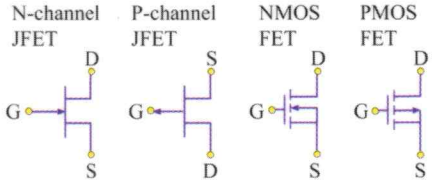


Figure 22

Approximate Low Frequency Equivalent Circuits

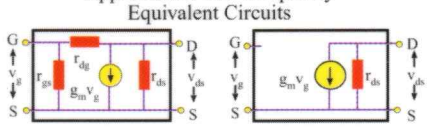


Figure 23

High Frequency Equivalent Circuit of a JFET

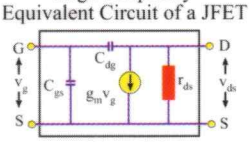


Figure 24

Current in an FET is carried by majority carriers drifting under the influence of an electric field, whereas in the bipolar transistor, current is transported by means of diffusing minority carriers. Since drift velocities in semiconductors are usually very much higher than diffusion velocities, carrier transit times are much shorter in FETs than in bipolar transistors. For this reason, one might expect FETs to have a much more extended high-frequency range than bipolar devices.

A limitation to the high-frequency performance or the switching speed of a FET is the gate-channel capacitance, which must be charged *via* the channel resistance. The resulting time constant determines the upper limit of the frequency response. The gain × bandwidth product, which can be derived from the equivalent circuit and equals $g_m/2\pi C_g$, is normally taken as a *figure of merit* to indicate the high-frequency response of a particular device. $\frac{g_m}{C_g} = \mu_e \frac{V_g - V_T}{L^2}$; $\mathbf{C_g}$: Total gate capacitance

COMMON-GATE AMPLIFIER

Common-gate (CG) FET amplifier circuit and its equivalent circuits Fig. 25

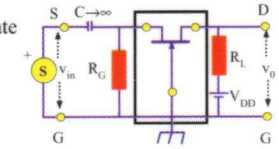
$$A_v = \frac{v_0}{v_{in}} = \frac{(\mu + 1)R_L}{r_d + R_L} \cong g_m R_L \text{ for}$$

$$\mu = g_m r_d >> 1, r_d >> R_L$$

$$R_i = \frac{v_{in}}{i_1} = \frac{R_L + r_d}{\mu + 1} \cong \frac{1}{g_m} \text{ for } r_d >> R_L;$$

$$R_0 = \frac{v_0}{i_2} = r_d + (\mu + 1)R_G \cong r_d + \mu R_G$$

Common-Gate Amplifier



(μ : Amplification factor)

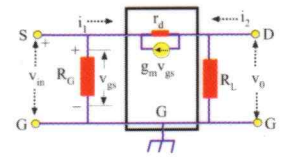


Figure 25

Note : For **CG** configuration, the output resistance is very large and can be considered as infinite; the input resistance is relatively low. Voltage gain is dependent on $\mathbf{R_L}$, and its maximum value is about μ . **CG** configuration in FET is the counterpart of **CB** configuration in BJTs.

COMMON-SOURCE AMPLIFIER

A common-source **(CS)** FET amplifier (with the dc biasing circuitry) and its small signal equivalent circuit are shown in Fig. 26.

Common-Source Amplifier

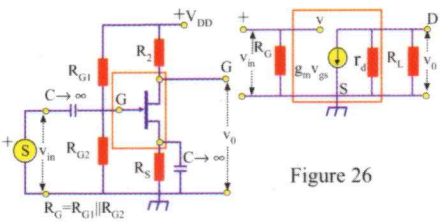


Figure 26

$$R_{in} \to \infty; R_0 = r_d; v_0 = -g_m (r_d \| R_L) v_{in}$$

$$A_v = \frac{v_0}{v_{in}} = -gm (r_d \| R_L) \cong -g_m R_L \text{ for } r_d >> R_L$$

$$\left(\frac{v_0}{v_{in}}\right)_{max} = -g_m r_d = \mu >> 1$$

COMMON-DRAIN AMPLIFIER

A common-drain **(CD)** FET amplifier (with the biasing circuitry) and its small-signal equivalent circuit are shown in Fig. 27.

Common-Drain Amplifier

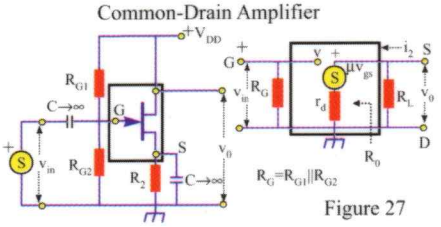


Figure 27

$R_{in} \to \infty$;

$$R_0 = \frac{v_0}{i_2} = \frac{r_d}{1 + \mu} \cong \frac{r_d}{\mu} = \frac{1}{g_m} \text{ for } \mu >> 1$$

$$A_v = \frac{v_0}{v_{in}} = \frac{\mu R_L}{(1 + \mu)R_L + r_d} \cong \frac{g_m R_L}{1 + g_m R_L}$$

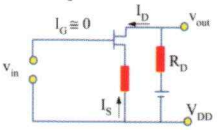
For $\mathbf{g_m R_L >> 1}$, the voltage gain is close to unity. The **CD** configuration is therefore called the *source follower* **(SF)**, since the source voltage follows the input gate signal. The **CS** configuration in FET is the counterpart of the **CC** configuration in BJT.

Summary on JFETs & MOSFETs

N-CHANNEL JFET

Figure 28

Common Source Amplifier

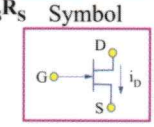


Parameters	
V_T	–
K	I_{DSS}/V_p^2
$\lambda \triangleq 1/V_A$	+
r_0	$\lvert V_A \rvert / I_D$
V_{DS}	+

$v_{in} = V_{GS} - I_S R_S$

$v_{out} = -V_D - I_D R_D = V_{DS} - I_S R_S$

Symbol



$$A_v = \frac{\Delta v_{out}}{\Delta v_{in}} = \frac{R_0}{R_0 + \frac{1}{g_m}}$$

- **On-State:** $v_{GS} > V_T$
- **Satration Region:** $v_{DS} \geq v_{GS} - V_T$

$$i_D = K(v_{GS} - V_T)^2(1 + \lambda V_{DS})$$

- **Triode Region:** $V_{DS} \leq V_{GS} - V_T$

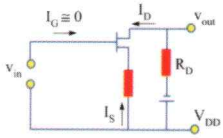
$$i_D = K[2(v_{GS} - V_T)v_{DS} - v^2_{DS}]$$

- **V_A: A FET Parameter**

P-CHANNEL JFET

Figure 29

Common Source Amplifier

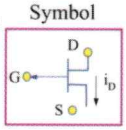


Parameters	
V_T	+
K	I_{DSS}/V_p^2
$\lambda \triangleq 1/V_A$	–
r_0	$\lvert V_A \rvert / I_D$
V_{DS}	–

$V_{in} = V_{GS} - I_S R_S$

$V_{out} = -V_{DD} - I_D R_D = V_{DS} - I_S R_S$

Symbol



$$A_v = \frac{\Delta v_{out}}{\Delta v_{in}} = \frac{R_0}{R_0 + \frac{1}{g_m}}$$

- **On-State:** $v_{GS} \leq V_T$
- **Satration Region:** $v_{DS} \leq v_{GS} - V_T$

$$i_D = K(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

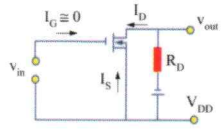
- **Triode Region:** $V_{DS} \geq V_{GS} - V_T$

$$i_D = K[2(v_{GS} - V_T)v_{DS} - v^2_{DS}]$$

N-CHANNEL DEPLETION MOSFET

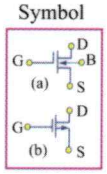
Figure 30

Common-Source Amplifier



Parameters	
V_T	–
K	$\mu_n C_{ox} \frac{W}{2L}$
Others	As for N-Channel JFET

Symbol



$v_{in} = V_{GS}$

$v_{out} = -V_{DD} - I_D R_D = V_{DS}$

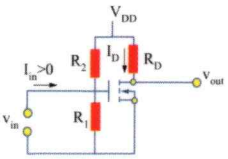
$$A_v = \frac{\Delta v_{out}}{\Delta v_{in}} \cong g_m R_D$$

(a) Conventional
(b) When substrate/body "B" connected to source
Note: Different states and regions of operation:
⇒ Same as for N-channel JFET

N-CHANNEL ENHANCEMENT MOSFET

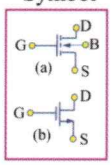
Figure 31

Common Source Amplifier



Parameters	
V_T	+
Others Parameters	As for N-Channel Depletion MOSFET

Symbol



$v_{in} = V_{GS}$

$v_{out} = V_{DD} - I_D R_D = V_{DS}$

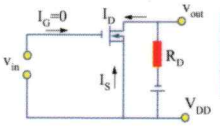
$$A_v = \frac{\Delta v_{out}}{\Delta v_{in}} \cong g_m R_D$$

(a) Conventional
(b) When substrate/body "B" connected to source
Note: Different states and regions of operation:
⇒ Same as for N-channel JFET

P-CHANNEL DEPLETION MOSFET

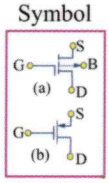
Figure 32

Common Source Amplifier



Parameters	
V_T	+
K	$\mu_p C_{ox} \frac{W}{2L}$

Symbol



μ_p: Hole mobility

$v_{in} = V_{GS}$

$v_{out} = -V_{DD} - I_D R_D = V_{DS}$

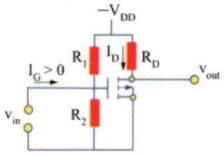
$$A_v = \frac{\Delta v_{out}}{\Delta v_{in}} \cong g_m R_D$$

(a) Conventional
(b) When substrate/body "B" connected to source
Note: Different states and regions of operation:
⇒ Same as for P-channel JFET

P-CHANNEL ENHANCEMENT MOSFET

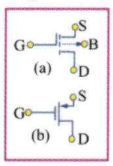
Figure 33

Common Source Amplifier



Parameters	
V_T	–
Other Parameters	As for P-Channel Depletion MOSFET

Symbol



$v_{in} = V_{GS}$

$v_{out} = V_{DD} - I_D R_D = V_{DS}$

$$A_v = \frac{\Delta v_{out}}{\Delta v_{in}} \cong g_m R_D$$

(a) Conventional
(b) When substrate/body "B" connected to source
Note: Different states and regions of operation:
⇒ Same as for P-channel JFET

COMPARISON OF FET AMPLIFIERS

	CG	CS	CD(SF)*
R_{in}	$1/g_m$	∞	∞
R_0	∞	r_d	$1/g_m$
$A_v = \frac{v_0}{v_{in}}$	$g_m R_L$	$-g_m R_L$	$\frac{g_m R_L}{g_m R_L + 1}$

*SF=Source Follower

OP-AMPS REVISITED

- **INSTRUMENTATION AMPLIFIER** - a high-performance differential amplifier with high-input impedance.
  - $V_0 = -(R_4/R_3)(1 + R_2/R_1)(V_1 - V_2)$
  - Input impedance presented at both inputs tends to be infinity.
  - Output impedance of the differential amplifier tends to be zero.
  - Application: To amplify differential signal(s) from transducers / sensors.
  - R_1 can be adjusted to achieve null-offset.

Common-Source Amplifier

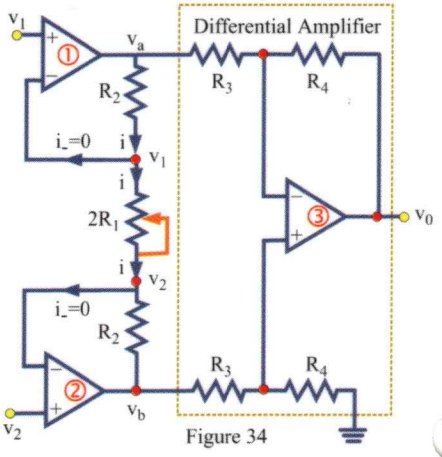


Figure 34

- **AC-COUPLED NON-INVERTING AMPLIFIER**:
  - Capacitively coupling an OP-AMP reduces the dc offset considerably.
  - Provision of R_3 is mandated to facilitate continuous dc path for each of the input terminals.

AC-Coupled Amplifier

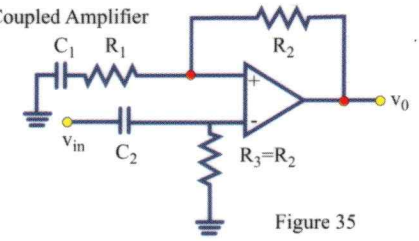


Figure 35

- **A SUMMARY ON OP-AMPS**
  - OP-AMPS in practical circuits offer performance matching theoretical estimations.
  - An OP-AMP consists of:

(a) An inverting input terminal;
(b) A non-inverting input terminal;
(c) An output terminal;
(d) Two power supply terminals + and –, with a common circuit ground.

  - Ideally, an OP-AMP responds to the two inputs ($+v_{in1}$) and ($-v_{in2}$) to yield an output $V_0 = A(v_{in1} - v_{in2})$; A is known as open-loop gain, which is very large (Ideally $A \rightarrow \infty$; in practice, $A \sim 10^4$ to 10^6).
  - An ideal OP-AMP has an infinite input impedance (at both input terminals) and a zero output impedance.
  - With a negative feedback, the closed-loop gains are:
- For inverting input, $v_o/v_{in1} = R_2 / R_1$
- For non-inverting input, $v_o/v_{in2} = (1 + R_2/R_1)$

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